Journal of Mechanical Engineering and Sciences (JMES)
ISSN (Print): 2289-4659; e-ISSN: 2231-8380; Volume 9, pp. 1614-1627, December 2015

DOI: http://dx.doi.org/10.15282/jmes.9.2015.9.0157

Optimization of process parameter variations on leakage current in in silicon-on-insulator vertical double gate mosfet device

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ABSTRACT

This paper presents a study of optimizing input process parameters on leakage current (I_{OFF}) in silicon-on-insulator (SOI) Vertical Double-Gate [1] Metal Oxide Field-Effect-Transistor (MOSFET) by using L36 Taguchi method. The performance of SOI Vertical DG-MOSFET device is evaluated in terms of its lowest leakage current (I_{OFF}) value. An orthogonal array [2], main effects, signal-to-noise ratio (SNR) and analysis of variance (ANOVA) are utilized in order to analyze the effect of input process parameter variation on leakage current (I_{OFF}). Based on the results, the minimum leakage current ((I_{OFF}) of SOI Vertical DG-MOSFET is observed to be 0.009 nA/μm or 9 ρA/μm while keeping the drive current (I_{ON}) value at 434 μA/μm. Both the drive current (I_{ON}) and leakage current (I_{OFF}) values yield a higher I_{ON}/I_{OFF} ratio (48.22 x 10^6) for low power consumption application. Meanwhile, polysilicon doping tilt angle and polysilicon doping energy are recognized as the most dominant factors with each of the contributing factor effects percentage of 59% and 25%.

Keywords: Analysis of variance; DG-MOSFET; SNR; SOI.

INTRODUCTION

The Metal Oxide Semiconductor Field-Effect-Transistor (MOSFET) with silicon-on-insulator (SOI) technology has been widely studied due to its superb device performance. The SOI technology has been proven to suppress short channel effects (SCE), thus improving the drive current (I_{ON}). The drive current (I_{ON}) is an important response to determine the driving capability of the MOSFET device. However, the leakage current (I_{OFF}) is still an important response to be controlled in order to obtain higher I_{ON}/I_{OFF} ratio. The high I_{ON}/I_{OFF} ratio will lead to lower power consumption of the device. Therefore, in pursuing excellent characteristics of SOI vertical DG-MOSFET device, the drive current (I_{ON}) must be ensured to be large while keeping the leakage current (I_{OFF}) as low as possible. Leakage current (I_{OFF}) is measured during the switch-off condition of the device. In other words, it is a value of drain current (I_D) when there is no gate voltage (V_G) applied [3]. Normally, as the device shrinks, the leakage current (I_{OFF}) will be higher. High leakage current (I_{OFF}) in nano-scale regimes is becoming a significant contributor to power dissipation of the MOSFET device [4]. This increase in I_{OFF} is typically due to charge sharing effect caused by drain-induced barrier lowering (DIBL) or due to deep channel punchthrough currents [5]. As the channel width decreases, both threshold

voltage (V_{TH}) and leakage current (I_{OFF}) will get modulated by the width of the transistor, giving rise to significant narrow-width effect. All these adverse effects will cause threshold voltage (V_{TH}) reduction (leakage current increase), especially in very small scaled devices [4]. Many factors are believed to have a large contribution to a rise of leakage current (I_{OFF}) value. One of the most recognized factors is known as process parameter variations. The input process parameters, such as V_{TH} implant dose, V_{TH} implant energy, polysilicon tilt angle, S/D implant energy and etcetera, need to be optimized in order to obtain a robust design. A lot of input process parameters have to be studied in order to identify the most significant factors that are influencing the leakage current (I_{OFF}) value. This paper attempts to describe the optimization of input process parameters for a minimum value of leakage current (I_{OFF}) in the SOI Vertical DG-MOSFET device. The responses of certain designs can be optimized by modeling the input process parameters [4, 6-9] . Sixteen input process parameters are involved in the analysis, which are substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, V_{TH} implant tilt, polysilicon doping dose, polysilicon doping energy, polysilicon doping tilt, halo implant dose, halo implant energy, halo implant tilt, S/D implant dose, S/D implant energy, S/D implant tilt, compensation implant dose, compensation implant energy and compensation implant tilt. Due to its large number of input process parameters, an orthogonal array of L_{36} is selected for this analysis.

The well-known statistical method known as Taguchi method is utilized in this analysis. The Taguchi approach provides a practical design strategy in which a modified design of experiment (DOE) is introduced. This technique emphasizes on reducing the number of experimental runs, but still increasing the efficiency. In the present study, there are mixed matrices of 16 input process parameters with 3 levels and 2 noise factors with 2 levels involved. There will be as many as 172,186,884 (316x22) runs of experiment if using the conventional full factorial design. The experiment will take only 144 runs with Taguchi method. Therefore, Taguchi method is capable of assisting designer to study the effect of many factors in the most economical way. A special orthogonal array consisting of 36 rows and 4 columns is constructed in order to retrieve 144 samples of result. This orthogonal array is used for design of experiment (DOE) that could assist the designer to study multiple process parameters variation in a fast and economic way. Signal-to-noise ratio (SNR) is utilized in order to analyze the data and then to figure out the optimal combination of process parameters [10]. There are three categories of performance characteristics in the analysis of SNR, which are known as nominal-the-better, lower-the-better and higher-the-better [11]. The SNR of each level of input process parameters is computed based on signal-to-noise (S/N) analysis. Regardless of the category of the performance characteristic, larger SNR corresponds to better performance characteristic [12, 13].

Therefore, the optimal level of the process parameters is the level with the highest SNR. In addition, a statistical analysis of variance (ANOVA) is conducted to observe which process parameters are statistically dominant and significant. With the SNR and ANOVA analysis, the optimal combination of the process parameters can be accurately predicted [14, 15]. Finally, a confirmation experiment is performed to verify the optimal process parameters obtained from the Taguchi analysis. Therefore, the Taguchi method is utilized to obtain the most optimal process parameters for lower I_{OFF} value of the device.

MATERIALS AND METHODS

SILVACO Technology Computer Aided Design (TCAD) tools are utilized to aid in designing and optimizing the input process parameters. SILVACO TCAD tools consist of two modules, which are ATHENA and ATLAS. ATHENA module was used for process simulation in the device's design. Meanwhile, ATLAS module was used for device simulation and characterization.

Process and Device Structure

The process began with a selection of a P-type silicon with <100> orientation as the main substrate. Initial silicon was then being doped with boron with concentration of 1 x 10^{14} atom/cm^3. The formation of BOX was done by depositing 40 nm oxide thickness (t_{BOX}). The silicon thickness [16] was about 4 nm. The silicon was dry etched in order to form a pillar or ridge that separates the two gates. The height of the silicon pillar of 140 nm was preferred in order to provide the effective channel length (L_{eff}) of 79 nm. The simulation process was followed by the gate oxidation process at a temperature of 875^o C. The thickness of gate oxide is a very essential parameter in vertical dimension, which will determine the gate control. Next step was to dope substrate ions which was boron into the silicon with concentration of 3.81 x 10^{11} atom/cm^3 at an energy level of 10 Kev and tilt angle of 7^o. This step is important in order to vary the threshold voltage (V_{TH}) of the vertical DG-MOSFET device. The next simulation process was to deposit polysilicon on top of the gate oxide. Then, the polysilicon and polysilicon oxide were etched away to form a gate polysilicon. The gate was made of polysilicon due to its ability to prevent source/drain ions from being penetrated into channel region. A layer of oxide was oxidized on top of polysilicon deposition at a temperature of 880 C^o. A phosphor dosage of 1 x 10^{18} atom/cm^3 was then dipped into the polysilicon gate at an energy level of 20 Kev and tilt angle of 10^o. This is done in order to increase the conductivity of the polysilicon since polysilicon is a low conductive metal. The conductivity of the gate would affect the switching frequency of the transistor.

In order to get an optimum performance for Vertical DG-MOSFET device, indium with a dosage of 1.17 x 10^{13} atom/cm^3 was doped at an energy level of 170 Kev and tilt angle of 24^o. Halo implantation was followed by depositing sidewall spacers. The sidewall spacers were then used as a mask for source/drain implantation. An arsenic atom with a concentration of 1.25 x 10^{18} atom/cm^3 at an energy level of 45 Kev and tilt angle of 80^o was implanted to ensure the smooth current flow in vertical DG-MOSFET device. Compensation implantation is utilized later by implanting phosphor dosage of 2.51 x 10^{12} atom/cm^3 at an energy level of 63 Kev and tilt angle of 7^o. This step is taken in order to reduce parasitic effects that could lower the current. Next, silicide (CoSi) was formed at the top of the source and drain region by sputtering cobalt on silicon surface. This transistor was then connected with aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [17-21]. The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened. It is important to use the same level of process parameters for both SOI and without SOI vertical DG-MOSFET device in order to investigate their performance. The final SOI vertical DG-MOSFET device structure was completed by mirroring the right-hand side structure. The completed structure of SOI Vertical DG-MOSFET device is illustrated in Figure 1. Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics such as the subthreshold drain

current (I_D) versus gate voltage (V_G). The off-state leakage current (I_{OFF}) can be extracted from that curve.

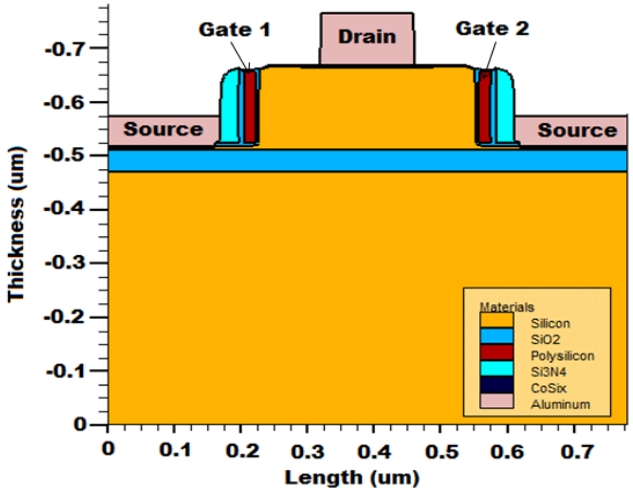

Figure 1. SOI vertical DG-MOSFET device structure.

Table 1. Input process parameters and their levels.

Symbol	Process Parameter	Units	Level 1	Level 2	Level 3
A	Substrate Implant Dose	atom/cm^3	1E14	1.03E14	-
B	V_{TH} Implant Dose	atom/cm^3	3.78E11	3.81E11	-
C	V_{TH} Implant Energy	kev	10	12	-
D	V_{TH} Implant Tilt	degree	7	10	13
E	Polysilicon Doping Dose	atom/cm^3	3.60E14	3.63E14	3.66E14
F	Polysilicon Doping Energy	kev	20	22	24
G	Polysilicon Doping Tilt	degree	7	10	13
H	Halo Implant Dose	atom/cm^3	1.17E13	1.20E13	1.23E13
J	Halo Implant Energy	kev	170	172	174
K	Halo Implant Tilt	degree	24	27	30
L	S/D Implant Dose	atom/cm^3	1.22E18	1.25E18	1.28E18
M	S/D Implant Energy	kev	43	45	47
N	S/D Implant Tilt	degree	74	77	80
O	Compensate Implant Dose	atom/cm^3	2.51E12	2.54E12	2.57E12
P	Compensate Implant Energy	kev	61	63	65
Q	Compensate Implant Tilt	degree	7	10	13

Taguchi Orthogonal L_{36} Array Design

The objective of the present study was to determine the optimal level of 16 input process parameters, i.e. substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, V_{TH} implant tilt, polysilicon doping dose, polysilicon doping tilt, halo implant dose, halo implant tilt, S/D implant dose and etc. Each of them were represented by A, B, C, D, E, F, G, H, J, K, L, M, N, O, P and Q. Two levels of the first 3 input process parameters and three levels of the other 13 input process parameters were selected as shown in Table 1. The presence of two noise factors, gate oxidation temperature and polysilicon oxidation temperature, were meant to put the undesirable effect (temperature) into design consideration. The values of noise factors at different levels are listed in Table 2.The

function of an orthogonal array is to reduce the number of experiments in identifying the most dominant factors in the design. The data produced from the experiment will be studied by using the S/N and ANOVA analysis. L_{36} (3^{16}) orthogonal array consists of 36 sets of experiment. The experimental layout of L_{36} (3^{16}) orthogonal array for the input process parameters is shown in Table 3.

Table 2. Noise Factors and Their Levels

Symbol	Noise factor	Units	Level 1	Level 2
U	Gate Oxidation Temperature	C^o	875	878
V	Polysilicon Oxidation Temperature	C^o	877	880

Table 3. Experimental Layout using L_{36} Orthogonal Array

Exp no.	Process Parameter Levels															
	A	B	C	D	E	F	G	H	J	K	L	M	N	O	P	Q
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	2
3	1	1	1	1	3	3	3	3	3	3	3	3	3	3	3	3
4	1	2	2	1	1	1	1	1	2	2	2	2	3	3	3	3
5	1	2	2	1	2	2	2	2	3	3	3	3	1	1	1	1
6	1	2	2	1	3	3	3	3	1	1	1	1	2	2	2	2
7	2	1	2	1	1	1	2	3	1	2	3	3	1	2	2	3
8	2	1	2	1	2	2	3	1	2	3	1	1	2	3	3	1
9	2	1	2	1	3	3	1	2	3	1	2	2	3	1	1	2
10	2	2	1	1	1	1	3	2	1	3	2	3	2	1	3	2
11	2	2	1	1	2	2	1	3	2	1	3	1	3	2	1	3
12	2	2	1	1	3	3	2	1	3	2	1	2	1	3	2	1
13	1	1	1	2	1	2	3	1	3	2	1	3	3	2	1	2
14	1	1	1	2	2	3	1	2	1	3	2	1	1	3	2	3
15	1	1	1	2	3	1	2	3	2	1	3	2	2	1	3	1
16	1	2	2	2	1	2	3	2	1	1	3	2	3	3	2	1
17	1	2	2	2	2	3	1	3	2	2	1	3	1	1	3	2
18	1	2	2	2	3	1	2	1	3	3	2	1	2	2	1	3
19	2	1	2	2	1	2	1	3	3	3	1	2	2	1	2	3
20	2	1	2	2	2	3	2	1	1	1	2	3	3	2	3	1
21	2	1	2	2	3	1	3	2	2	2	3	1	1	3	1	2
22	2	2	1	2	1	2	2	3	3	1	2	1	1	3	3	2
23	2	2	1	2	2	3	3	1	1	2	3	2	2	1	1	3
24	2	2	1	2	3	1	1	2	2	3	1	3	3	2	2	1
25	1	1	1	3	1	3	2	1	2	3	3	1	3	1	2	2
26	1	1	1	3	2	1	3	2	3	1	1	2	1	2	3	3
27	1	1	1	3	3	2	1	3	1	2	2	3	2	3	1	1
28	1	2	2	3	1	3	2	2	2	1	1	3	2	3	1	3
29	1	2	2	3	2	1	3	3	3	2	2	1	3	1	2	1
30	1	2	2	3	3	2	1	1	1	3	3	2	1	2	3	2
31	2	1	2	3	1	3	3	3	2	3	2	2	1	2	1	1
32	2	1	2	3	2	1	1	1	3	1	3	3	2	3	2	2
33	2	1	2	3	3	2	2	2	1	2	1	1	3	1	3	3
34	2	2	1	3	1	3	1	2	3	2	3	1	2	2	3	1
35	2	2	1	3	2	1	2	3	1	3	1	2	3	3	1	2
36	2	2	1	3	3	2	3	1	2	1	2	3	1	1	2	3

RESULTS AND DISCUSSION

After the process simulation was done by using ATHENA module, the designed device was then characterized by utilizing ATLAS module. In this section, the electrical characteristics of the first set of experiments will be discussed. Finally, the optimization approach using Taguchi method is discussed in detail.

Device Characterization

Figure 2 shows the graph of the subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05V and V_D = 1.0V for SOI vertical DG-MOSFET device. The value of off-leakage current (I_{OFF}) and drive current (I_{ON}) can be extracted from the graph. From the graph, it was observed that the value of drive current (I_{ON}) was at 474 µA/µm. The high drive current (I_{ON}) is required for high speed switching operation. The I_{ON} is the maximum drain current (I_{DMAX}) when V_{GS}=V_{DD} and V_{DS}=V_{DD}. Meanwhile, the off-leakage current (I_{OFF}) was observed to be at 0.024 x 10^{-9} A/ µm. The I_{OFF} is defined as a drain to source current and it is measured when V_{GS}=0 and V_{DS}= V_{DD}. In other words, the off-state current (I_{OFF}) is the drain current when no gate voltage is applied. The off-leakage current (I_{OFF}) was the electrical characteristic that had been optimized by using Taguchi method.

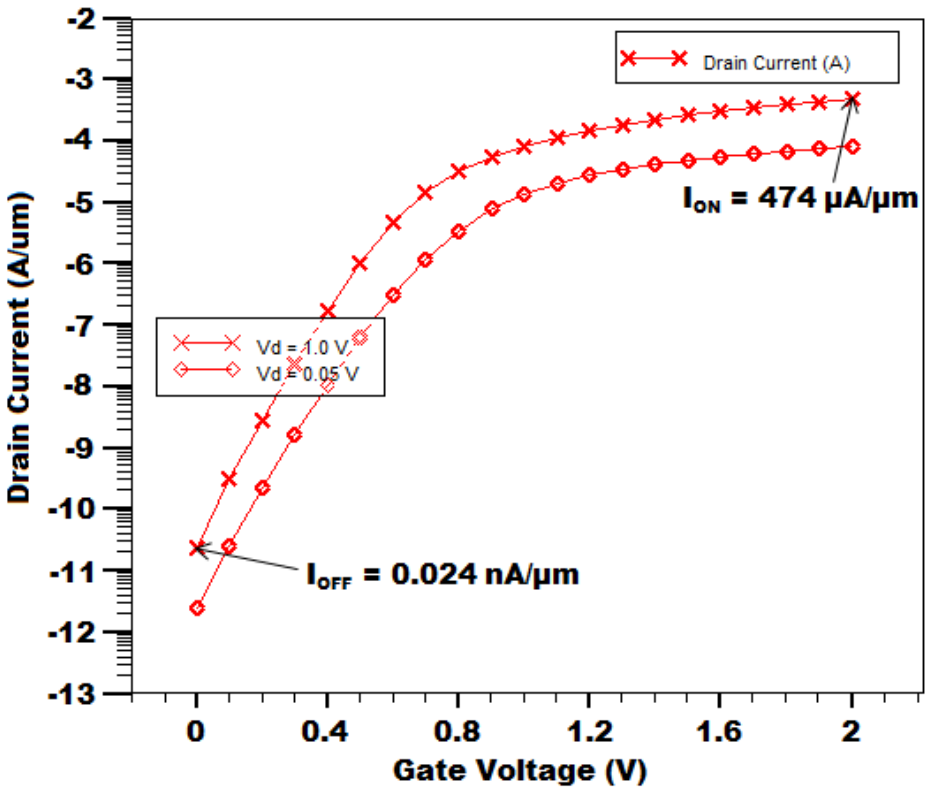

Figure 2. Graph of subthreshold drain current (I_D) versus gate voltage (V_G)

Leakage Current (I_{OFF}) Acquisition

The experimental results for I_{OFF} in SOI Vertical DG-MOSFET device are shown in Table 4. Each set of experiment produced four different I_{OFF} values due to the presence of two noise factors, which are factor U (Gate Oxidation Temperature) and factor V (Polysilicon Oxidation Temperature).

Table 4. I_{OFF} values for SOI vertical DG-MOSFET device.

Experiment no.	Leakage Current, I_{OFF} (nA/μm)			
	I_{OFF1} (U_1V_1)	I_{OFF2} (U_1V_2)	I_{OFF3} (U_2V_1)	I_{OFF4} (U_2V_2)
1	0.024	0.017	0.020	0.014
2	12.965	9.108	11.027	7.49
3	7799.56	5704.11	7202.73	5234.88
4	0.027	0.020	0.022	0.016
5	3.722	2.450	3.128	2.092
6	7096.08	4826.54	6520.6	4349.59
7	0.259	0.184	0.201	0.142
8	1044.71	717.9	900.67	638.0
9	1.298	0.775	1.073	0.662
10	42.661	22.998	36.374	18.758
11	0.070	0.045	0.057	0.037
12	297.33	224.70	264.64	199.79
13	576.65	425.39	507.22	372.93
14	0.946	0.523	0.808	0.442
15	0.253	0.148	0.192	0.111
16	482.03	345.76	418.98	297.89
17	1.234	0.728	1.041	0.615
18	0.318	0.219	0.256	0.174
19	0.029	0.022	0.025	0.019
20	287.05	209.61	256.36	185.29
21	22.985	12.753	18.763	10.234
22	11.423	7.076	9.046	5.975
23	8331.52	5985.85	7669.64	5480.76
24	0.017	0.012	0.014	0.01
25	298.31	220.02	261.72	197.37
26	16.58	8.529	12.799	7.01
27	0.052	0.04	0.045	0.035
28	121.01	87.213	105.61	75.471
29	12.506	6.758	9.985	5.313
30	0.076	0.045	0.064	0.038
31	6575.38	4703.25	5863.8	4307.13
32	0.022	0.016	0.017	0.012
33	20.504	13.763	17.33	11.519
34	1.571	0.853	1.321	0.727
35	0.22	0.15	0.177	0.117
36	515.85	372.67	449.27	322.55

Signal-to-noise (S/N) Response Analysis

After the results of 36 experiments have been obtained by utilizing SILVACO TCAD tools, the next step is to implement S/N response analysis. The objective of the S/N response analysis is to determine the signal-to-noise ratio (SNR) for every input process parameters. SNR is used to figure out the optimal input process parameters and analyze experimental data. For the S/N response analysis for I_{OFF}, category of the lower-the-better

is selected due to its ability to reduce the response value as minimum as possible. The SNR (lower-the-better), η can be expressed as [22]:

$$\eta = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n} y_i^2\right] \quad (1)$$

where *n* is the number of tests and *yi* is the experimental values of $I_{OFF.}$ The S/N ratio (lower-the-better) of each experiment was computed and recorded in Table 5 [22].

Table 5. Mean sum of SQ and S/N ratio for $I_{OFF.}$

Exp no.	Mean Sum of SQ	S/N Ratio (lower-the-better) [23]
1	0.0004	34.374
2	107.19	-20.301
3	4E+07	-76.351
4	0.0005	33.305
5	8.5042	-9.2963
6	3E+07	-75.286
7	0.0404	13.939
8	706262	-58.49
9	0.9688	0.1379
10	1005.9	-30.026
11	0.0029	25.397
12	62211	-47.939
13	227458	-53.569
14	0.5042	2.9742
15	0.0338	14.714
16	154046	-51.877
17	0.8787	0.5618
18	0.0612	12.131
19	0.0006	32.383
20	56597	-47.528
21	286.93	-24.578
22	74.521	-18.723
23	5E+07	-76.86
24	0.0002	37.393
25	61212	-47.868
26	140.15	-21.466
27	0.0019	27.239
28	9774.7	-39.901
29	82.5	-19.165
30	0.0033	24.769
31	3E+07	-74.709
32	0.0003	35.328
33	260.71	-24.162
34	1.3673	-1.3587
35	0.029	15.379
36	177717	-52.497

The effect of each input process parameter on the S/N ratio at different levels was separated because the experimental design is orthogonal. The S/N ratio (SNR) for each of the process parameter is summarized in Table 6. Normally, a larger SNR will result in a lower value of leakage current (I_{OFF}). The effect of each input process parameter on the S/N ratio at different levels was separated because the experimental design is orthogonal. In addition, the overall mean SNR for the 36 experiments is also calculated and listed in Table 6. Basically, the larger the S/N ratio will result in better quality characteristic for leakage current [10]. The higher the quality characteristic value to the target, the better the device quality will be [12]. It is crucial that the effort must be focused on reducing sensitivity to noise by optimizing SNR.

Table 6. S/N response for I_{OFF}.

Symbol	Process Parameter	S/N ratio (Lower-the-better)		
		Level 1	Level 2	Level 3
A	Substrate Implant Dose	-14.72	-16.5	-
B	V_{TH} Implant Dose	-16	-15.22	-
C	V_{TH} Implant Energy	-16.08	-15.14	-
D	V_{TH} Implant Tilt	-17.54	-14.41	-14.87
E	Polysilicon Doping Dose	-17	-20.11	-9.713
F	Polysilicon Doping Energy	2.7877	-9.271	-9.713
G	Polysilicon Doping Tilt	21.042	-22.29	-45.58
H	Halo Implant Dose	-14.75	-15.2	-16.87
J	Halo Implant Energy	-21.24	-11.59	-13.99
K	Halo Implant Tilt	-10.79	-16.07	-19.97
L	S/D Implant Dose	-22.38	-9.94	-14.5
M	S/D Implant Energy	-16.23	-20.03	-10.57
N	S/D Implant Tilt	-8.726	-15.04	-23.07
O	Compensation Implant Dose	-9.152	-15.05	-22.63
P	Compensation Implant Energy	-19.34	-10.42	-17.06
Q	Compensation Implant Tilt	-16.39	-21.84	-8.603

Analysis of Variance (ANOVA)

The objective of the analysis of variance (ANOVA) is to find out which input process parameters contributes the most significant impact on leakage current (I_{OFF}). Basically, it computes parameters known as sum of squares (SS), degree of freedom (DF), variance, F-value and percentage of each factor. The results of ANOVA for the SOI Vertical DG-MOSFET device are shown in Table 7. According to these analyses, the most dominant factors for SNR are factor G (Polysilicon doping tilt=59%) and factor F (Polysilicon doping energy=25%). Therefore, these factors should be set at 'best setting'. Meanwhile, the remaining factors will be considered as neutral or negligible factors. Therefore, they do not contribute large effect on the output response. The neutral factors level can be adjusted if the leakage current (I_{OFF}) value is not small as expected. The percentage of factor effect on SNR indicates the priority of a factor (process parameter) to reduce variation. The Pareto plot of standardized effect of I_{OFF} for SOI Vertical DG-MOSFET device is shown in Figure 3. The Pareto plot compares the relative magnitude and the statistical significance of all the main effects and ranks of parameter accordingly.

Table 7. Results of ANOVA for I_{OFF}.

Process Parameters	DF	SS	MS	F-value	Factor effect on SNR (%)
A	1	28	28	60	0
B	1	5	5	11	0
C	1	8	8	17	0
D	2	69	34	73	0
E	2	648	3421	722	1
F	2	11885	5943	12548	25
G	2	27436	13718	28966	59
H	2	30	15	32	0
J	2	606	303	640	1
K	2	509	255	538	1
L	2	951	475	1004	2.04
M	2	544	272	574	1
N	2	1240	620	1309	3
O	2	1095	547	1156	2
P	2	516	83	545	1
Q	2	1062	129	1121	2

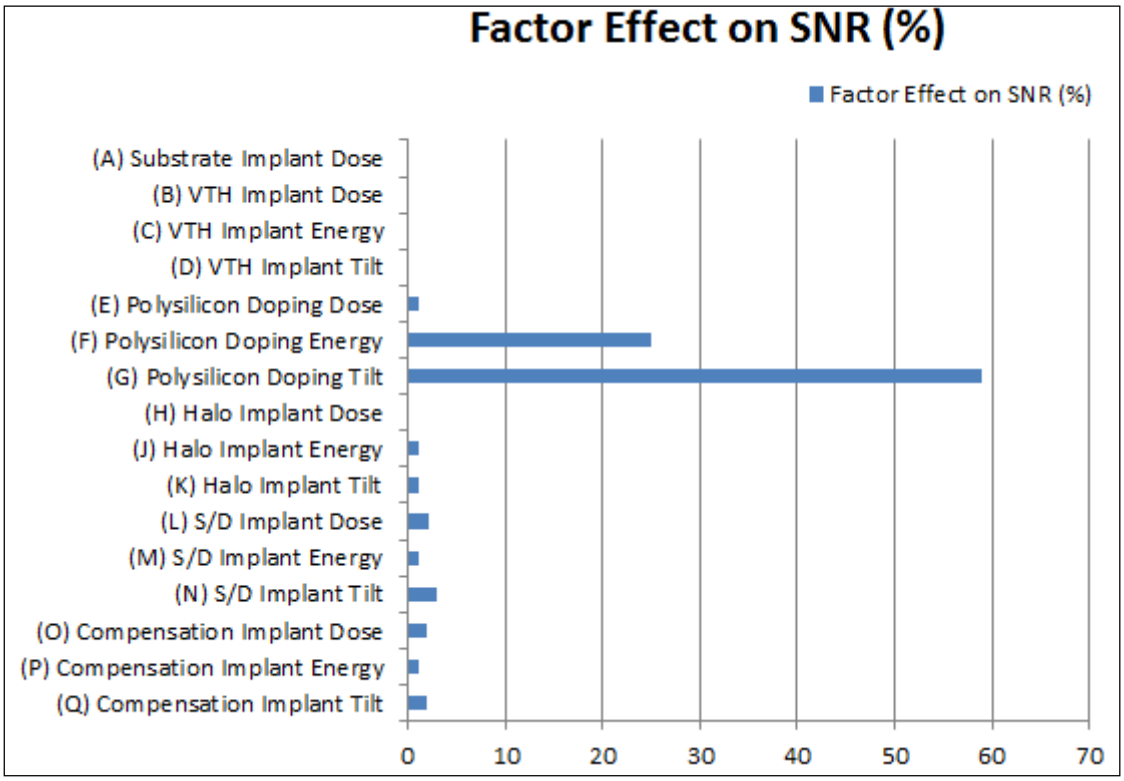

Figure 3. Pareto plot of I_{OFF} for SOI vertical DG-MOSFET sevice.

From Figure 3, it is obvious that output response I_{OFF}, factor G (Polysilicon doping tilt=59%) and factor F (Polysilicon doping energy=25%) were the most significant parameters. Since the factor G and factor F were fixed to level 1, the other input process parameters were varied in order to get an optimum result. After a few adjustments were made on the level of process parameters, the best level setting of process parameters was

identified as A1, B2, C2, D2, E1, F1, G1, H1, J2, K1, L1, M3, N1, O1, P1 and Q3. Factor A, B, C, D, E, F, G, H, J, K, L, M, N, O, P and Q each represents substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, V_{TH} implant tilt, polysilicon doping dose, polysilicon doping energy, polysilicon doping tilt, halo implant dose, halo implant energy, halo implant tilt, S/D implant dose, S/D implant energy, S/D implant tilt, compensation implant dose, compensation implant energy and compensation implant tilt respectively.

Confirmation Experiment for Response, I_{OFF}

The confirmation experiment is used to verify the expected results with the experimental results. The best setting of input process parameters for SOI Vertical DG-MOSFET device which were suggested by Taguchi method is shown in Table 8. The confirmation experiment is required in the device design because the optimum combination of parameters and their levels, i.e. A1, B2, C2, D2, E1, F1, G1, H1, J2, K1, L1, M3, N1, O1, P1 and Q3 do not correspond to any experiment of the orthogonal array.

Table 8. Best setting of process parameters.

Symbol	Process Parameter	Units	Best Value
A	Substrate Implant Dose	atom/cm^3	1x10^{14}
B	V_{TH} Implant Dose	atom/cm^3	3.81x10^{11}
C	V_{TH} Implant Energy	kev	12
D	V_{TH} Implant Tilt	degree	10
E	Polysilicon Doping Dose	atom/cm^3	3.60x10^{14}
F	Polysilicon Doping Energy	kev	20
G	Polysilicon Doping Tilt	degree	7
H	Halo Implant Dose	atom/cm^3	1.17x10^{13}
J	Halo Implant Energy	kev	172
K	Halo Implant Tilt	degree	24
L	S/D Implant Dose	atom/cm^3	1.22x10^{18}
M	S/D Implant Energy	kev	47
N	S/D Implant Tilt	degree	74
O	Compensation Implant Dose	atom/cm^3	2.51x10^{12}
P	Compensation Implant Energy	kev	61
Q	Compensation Implant Tilt	degree	13

The result of the final simulation for the device is shown in Table 9. Before the optimization approaches, the best SNR (Lower-the-better) is 37.393 dB at row of experiment no. 24 (refer to Table 5). After the optimization approaches, the SNR (Lower-the-better) of leakage current (I_{OFF}) for SOI Vertical DG-MOSFET device is 39.44 dB, which is higher than any values in Table 5. Hence, it is proven that the selected level of input process parameters are the optimum level setting (The highest SNR). In addition, these values are still within the predicted range. For S/N ratio (Lower-the-better), 39.44 dB is within predicted range S/N ratio of 19.73 to 59.15 dB (39.44 ± 19.71 dB). These indicate that Taguchi method is able to predict the optimum solution in finding the SOI Vertical DG-MOSFET device fabrication recipe with lowest leakage current value. The leakage current (I_{OFF}) value for the device after was observed to be 0.009 nA/μm or 9 ρA/μm as highlighted in Table 9. This leakage current (I_{OFF}) value was observed to be the lowest value among all the experiments done before.

Table 9. Results of confirmation experiments for I_{OFF}

Leakage Current, I_{OFF} (nA/μm)				SNR (Lower-the-better)
I_{OFF1} (U_1V_1)	I_{OFF2} (U_1V_2)	I_{OFF3} (U_2V_1)	I_{OFF4} (U_2V_2)	
0.016	0.012	0.013	0.009	39.44 dB

CONCLUSIONS

In conclusion, the optimum solution in designing SOI Vertical DG-MOSFET device with lowest leakage current (I_{OFF}) value was successfully predicted by utilizing L_{36} orthogonal array [2] of Taguchi method. Leakage current (I_{OFF}) is the main response studied in this project as it is one of the main factors that affect the power consumption of the device. Leakage current (I_{OFF}) must be as low as possible while keeping the drive current (I_{ON}) value at a high level. This will result in higher I_{ON}/I_{OFF} ratio, thereby lowering the power consumption of the device. Taguchi method design is used to develop a systematic design of experiment. It has many variants that can be applied to model the device and a lot of input process parameters can be analyzed. The level of significance of each input process parameters on leakage current (I_{OFF}) is determined by using ANOVA. Based on the ANOVA method, the most dominant input process parameters on leakage current (I_{OFF}) were factor G (Polysilicon doping tilt=59%) and factor F (Polysilicon doping energy=25%). The leakage current (I_{OFF}) value after the optimization approach was 0.009 nA/μm or 9 ρA/μm while keeping the drive current (I_{ON}) value at 434 μA/μm. Both the drive current (I_{ON}) and leakage current (I_{OFF}) values yield a higher I_{ON}/I_{OFF} ratio (48.22 x 10^6) for lower power consumption application.

ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Higher Education (MOHE) and Centre for Telecommunication Research and Innovation (CeTRI), Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for sponsoring this research study under the research grants (PJP/2014/FKEKK(6B)/S01341) and FRGS(RACE)/2012/FKEKK/TK02/02/2 F00148.

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